Amendments to the Claims:

Please cancel Claims 1-33 without prejudice.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-33. (canceled)

34. (previously presented) A bus architecture for a digital transceiver comprising:

a high speed bi-directional bus for communicating digital information thereon;

a first encryption/decryption unit (EDU) coupled to the bus for providing decrypted digital signals to a first functional unit from the bus and for providing encrypted digital signals to the bus from the first functional unit;

a second EDU coupled to the bus for providing decrypted digital signals to a second functional unit from the bus and for providing encrypted digital signals to the bus from the second functional unit; and

a controller for controlling transmission of digital signals on the bus wherein audio video signals are transmitted between the first and second EDUs

in encrypted form, the controller also for establishing encryption/decryption keys for the first and second EDUs and without exposing an unencrypted data stream.

35. (original) The architecture of Claim 34 wherein the first functional unit is an audio video decode block for decoding a data stream from a digital broadcast signal.

36. (original) The architecture of Claim 34 wherein the second functional unit is a graphics block for generating a video signal from the audio video digital signals received from the first functional unit.

37. (original) The architecture of Claim 34 wherein the controller is a CPU.

38. (original) The architecture of Claim 34 wherein the encryption process is key-based encryption process and the controller manages the distribution of keys to the first encryption unit and the second encryption unit.

39. (original) The architecture of Claim 34 further comprising an arbiter coupled to the controller for arbitration of the bus.

40. (original) The architecture of Claim 34 wherein the first functional unit, second functional unit, and third functional unit include respective identification registers for identifying each functional unit.

41. (original) The architecture of Claim 34 wherein the audio video digital signals are encrypted using an encryption process substantially compliant with DES ECB (Data Encryption Standard Electronic Code Book).

42. (original) The architecture of Claim 34 wherein the bus is a PCI (Peripheral Component Interconnect) compliant bus.

43. (original) The architecture of Claim 34 further comprising a front end block coupled to the bus for receiving a digital broadcast signal and generating the audio video digital signals therefrom, the first functional unit coupled to receive the audio video signals from the front end block via the bus.

44. (original) The architecture of Claim 34 wherein the audio video digital signals are substantially compliant with a version of the MPEG (Moving Pictures Experts Group) format.

45. (new) A transceiver system for receiving content contained in a secure digital broadcast signal, comprising:

a high speed bi-directional bus for communicating digital information thereon;

a first encryption/decryption unit (EDU) coupled to said bus for providing decrypted digital signals to a first functional unit from said bus and for providing encrypted digital signals to said bus from said first functional unit;

a second EDU coupled to said bus for providing decrypted digital signals to a second functional unit from said bus and for providing encrypted digital signals to said bus from said second functional unit; and

a controller for controlling transmission of digital signals on said bus wherein audio video signals are transmitted between said first and second EDUs in encrypted form, said controller also for establishing encryption/decryption keys for said first and second EDUs and without exposing an unencrypted data stream.

46. (new) The transceiver system of Claim 45 wherein said transceiver is a set-top box.

47. (new) The transceiver system of Claim 45 wherein said first functional unit is an audio video decode block for decoding said data stream from said digital broadcast signal.

48. (new) The transceiver system of Claim 45 wherein said second functional unit is a graphics block for generating said video signal from said data stream received from said first functional unit.

49. (new) The transceiver system of Claim 45 wherein said controller is a CPU (central processing unit) block coupled to said bus for managing an encryption process of said first encryption unit and said second encryption unit.

50. (new) The transceiver system of Claim 49 wherein the encryption process is key-based encryption process and said CPU block manages the distribution of keys to said first encryption unit and said second encryption unit.

51. (new) The transceiver system of Claim 49 further comprising an arbiter coupled to said CPU block for arbitration of said bus.

52. (new) The transceiver system of Claim 45 wherein the encryption process is key-based encryption process and said controller manages the distribution of keys to said first encryption unit and said second encryption unit.

53. (new) The transceiver system of Claim 45 further comprising an arbiter coupled to said controller for arbitration of said bus.

54. (new) The transceiver system of Claim 45 wherein said first functional unit, second functional unit, and third functional unit include respective identification registers for identifying each functional unit.

55. (new) The transceiver system of Claim 45 wherein said data stream encrypted using an encryption process substantially compliant with DES ECB (Data Encryption Standard Electronic Code Book).

56. (new) The transceiver system of Claim 45 wherein said bus is a PCI (Peripheral Component Interconnect) compliant bus and each encryption unit performs encryption and decryption.

57. (new) The transceiver system of Claim 45 further comprising a front end block coupled to said bus for receiving said digital broadcast signal and generating said data stream therefrom, said first functional unit coupled to receive said data stream from said front end block via said bus.

58. (new) The transceiver system of Claim 45 wherein said data stream is substantially compliant with a version of the MPEG (Moving Pictures Experts Group) format.

59. (new) In a set-top box transceiver, a high security bus architecture for implementing secure transmission of data between components of said transceiver, comprising:

a high speed bi-directional bus for communicating digital information thereon;

a first encryption/decryption unit (EDU) coupled to said bus for providing decrypted digital signals to a first functional unit from said bus and for providing encrypted digital signals to said bus from said first functional unit;

a second EDU coupled to said bus for providing decrypted digital signals to a second functional unit from said bus and for providing encrypted digital signals to said bus from said second functional unit; and

a controller for controlling transmission of digital signals on said bus wherein audio video signals are transmitted between said first and second EDUs in encrypted form, said controller also for establishing encryption/decryption keys for said first and second EDUs and without exposing an unencrypted data stream.

60. (new) The architecture of Claim 59 wherein said first functional unit and said first encryption unit are built into a first integrated circuit device and said second functional unit and said second encryption unit are built into a second integrated circuit device.

61. (new) The architecture of Claim 59 wherein said first functional unit is an audio video decode block for decoding said data stream from an external source.

62. (new) The architecture of Claim 59 wherein said second functional unit is a graphics block for generating a video signal from said data stream received from said first functional unit.

63. (new) The architecture of Claim 59 wherein said first functional unit is a conditional access block for descrambling a digital broadcast signal.

64. (new) The architecture of Claim 59 wherein said second functional unit is an audio video decode block for decoding said data stream received from said first functional unit.

65. (new) The architecture of Claim 59 wherein said controller is a CPU (central processing unit) block coupled to said bus for managing an encryption process of said first encryption unit and said second encryption unit.

66. (new) The architecture of Claim 65 wherein the encryption process is key-based encryption process and said CPU block manages the distribution of keys to said first encryption unit and said second encryption unit via said bus.

67. (new) The architecture of Claim 65 further comprising an arbiter coupled to said CPU block for arbitration of said bus.

68. (new) The architecture of Claim 65 wherein said first functional unit, second functional unit, and third functional unit include respective identification registers for implementing component identification via said bus.

69. (new) The architecture of Claim 65 wherein said data stream is encrypted using an encryption process substantially compliant with DES ECB (Data Encryption Standard Electronic Code Book).

70. (new) The architecture of Claim 65 wherein said bus is a PCI (Peripheral Component Interconnect) compliant bus and provides bi-directional communication between said first functional unit and said second functional unit.

71. (new) The architecture of Claim 59 wherein the encryption process is key-based encryption process and said controller manages the distribution of keys to said first encryption unit and said second encryption unit via said bus.

72. (new) The architecture of Claim 59 further comprising an arbiter coupled to said controller for arbitration of said bus.

73. (new) The architecture of Claim 59 wherein said first functional unit, second functional unit, and third functional unit include respective identification registers for implementing component identification via said bus.

74. (new) The architecture of Claim 59 wherein said data stream is encrypted using an encryption process substantially compliant with DES ECB (Data Encryption Standard Electronic Code Book).

75. (new) The architecture of Claim 59 wherein said bus is a PCI (Peripheral Component Interconnect) compliant bus and provides bi-directional communication between said first functional unit and said second functional unit.

76. (new) The architecture of Claim 59 further comprising a front end block coupled to said bus for receiving said digital broadcast signal and generating said data stream therefrom, said first functional unit coupled to receive said data stream from said front end block via said bus.

77. (new) The architecture of Claim 59 wherein said data stream is substantially compliant with a version of the MPEG (Moving Pictures Experts Group) format.